Litho World: First International Workshop on Advanced Patterning Solutions (IWAPS)

First International Workshop on Advanced Patterning Solutions (IWAPS) held on October 12-13, 2017 was a great success with a record number of 21 speakers and over 200 attendees from around the world. This workshop was held under the auspices of the Integrated Circuit Industry Technology Innovation Alliance in China (ICTIA), undertaken by Institute of Microelectronics of Chinese Academy of Science (IMECAS) and sponsored by SMIC, YMTC, Huahong Group, Mentor, ASML, KLA Tencor, Nata, SMEE, Synopsys, Toppan, JSR, DJEL and KINGSEMI.

At the beginning of the workshop, Jianlin Cao (president of IWAPS, chairman of ICTIA, former vice minister of Ministry of Science and Technology), Junru Ma (the former director of the Bureau of the State Administration of Foreign Experts) and Gang Qiu (deputy inspector of Key Special Affairs Office of Ministry of Science and Technology, vice director of 02 Special Implementation Management Office) made the opening speech for the workshop successively. Tianchun Ye, vice president of IWAPS and director of IMECAS, made an analysis report about current industry trends.

Secretary general of IWAPS Yayi Wei who is also the director of Computational Lithography R&D Center in IMECAS presided over the opening ceremony. Professors, fellows, managers and engineers from intel, IBM, Qualcomm, AMD, ASML, SMIC and so on were invited to make reports about computational lithography technology toward 7nm and below, SMO, DTCO, EUV, DSA, Design rules, Advanced Lithography Material, lithography equipment, etc.

The Workshop provides an environment where leading researchers and engineers from various disciplines in patterning can share their thoughts and ideas. The speakers at the Workshop are selected by invitation only and represent a broad range of disciplines and covering a wide array of different lithography approaches and requirements. Presentations are arranged to be comprehensive, covering the current practice, the future trend and the challenges ahead. The Workshop format is to provide an atmosphere for in-depth discussions among the attendees. This workshop also provides an opportunity for researchers and engineers who want to know more about the semiconductor R&D and business opportunity in China.

The following are the details of this workshop.

▲Jianlin Cao (president of IWAPS, chairman of ICTIA, former vice minister of Ministry of Science and Technology)

▲Junru Ma (the former director of the Bureau of the State Administration of Foreign Experts)

▲Gang Qiu (deputy inspector of Key Special Affairs Office of Ministry of Science and Technology, vice director of 02 Special Implementation Management Office)

▲Tianchun Ye (vice president of IWAPS, director of IMECAS)

▲Yayi Wei (Secretary general of IWAPS, director of Computational Lithography R&D Center in IMECAS)

Material

Wang Yueh a program manager and principal engineer working on advance materials for future generations. The title of his report is “Current and Future Litho Patterning Materials: Challenges and Expectations”. In this talk, the current ArF patterning materials status and what the challenges and opportunities for sub-10nm generations is presented. Also, EUVL has been transitioned from

the research phase to full development phase - with integrated testing of the various technology components: exposure tools, masks, and resists. It is very challenges for resists to meet the material targets specification (MTS), especially when we shrink the CD into single-digital nm in the future. From this talk, the Intel end-user views and expectations for future generation materials is provided.

Toru KIMURA is a research director of JSR Corporation and has responsibility for semiconductor materials development. The title of his report is "Advanced Lithography Material Status toward 7nm Node and Beyond". This talk reported JSR is developing functional spin-on multi-layers, which are spin-on carbon hard mask and spin-on Si materials. There are advantages about process margin at patterning step and etching step. And, 13.5nm lithography has been recognized as a promising candidate for the manufacturing of semiconductor devices for 7nm node and beyond. For the high volume manufacturing of semiconductor devices, significant improvement of sensitivity and line edge roughness (LWR) and Local CD Uniformity (LCDU) is required for 13.5nm resist. The recent progress of sensitivity and LWR/LCDU improvement of JSR novel 13.5nm resist and process is reported.

Process

Dr. Deng Hai currently serves as a full professor in the Polymer Department of Fudan University. The title of his report is "Ultrafast Sub-5 nm DSA at Low Temperature". In this report, a new high x DSA copolymers for fast assembling under 100℃ is designed. Through the SAXs, TEM and SEM, such new DSA systems achieved resolution of 4.4 nm or less, after 1 min at 80℃ thermal annealing are demonstrated.

Lijun Chen is currently the deputy division director of Engineering III Division at HLMC. The title of his report is "Systematic Experimental Study on Stitching Techniques of CMOS Image Sensors". In this talk, the systematic experimental study on stitching technology of CMOS image sensors is shown. The main difficulties and solutions of stitching technology include making stitching scheme, optimizing the chip layout, defining the design rules, optimizing the layout design and monitoring the equipment. The proposed sensor was designed and implemented on a 0.055μm CMOS process with stitching techniques. A CIS, 28.3mm × 38.8mm, 42 Mega pixels, had been demonstrated on 12 inch silicon wafer. Meanwhile, in order to verify the feasibility and capability, 203(v.) ×179(h.) mm2, almost the biggest sensor can be made on the 12 inch wafer, ~ 1.8 Billion pixels CIS was also demonstrated.

Kenjiro Nawa is a member of Process Integration Center at TEL. The title of his report is "Atomic Layer Approach for Advanced Patterning Technology". This presentation will provide an overview of the latest integrated process technologies and how atomic scale plasma processes can be used to overcome patterning limits at sub-10nm generation.

EUV

Shinji Kunitani is Technology Transfer Manager at Engineering Department, Toppan Photomasks Ltd. Shanghai. The title of his report is "Latest Optical and EUV Masks". As photomask for next generation lithography, Toppan is developing on both side of ArF Immersion and EUV. Advanced EB writer was introduced last year, and the mask process up to the 10nm node was completed. Currently we are developing the new technology from material to guarantee with target of 5nm–7nm. In this paper, current technical development status and our challenges are reported.

Dr. Akiyoshi Suzuki is a technical advisor at Gigaphoton. The title of his report is "Present Status of High-power LPP-EUV Source for HVM". In this talk, Gigaphonton's unique and original technologies is described, such as combination of pulsed CO2 laser and Sn droplets, dual

wavelength laser-pulse-shooting and debris mitigation with super-conducting magnets have broken the hard barriers over the years. Now, Gigaphonton has come to the development stage of the HVM EUV light source for the first time. The first EUV light source of Gigaphoton for HVM is now under construction. The promising intermediate data is shown. The 100W level output power has already been achieved. As for the availability, the lifetime of a collector mirror is of special concern, because it is one of the most important components for low cost operation. Systematic optimization with SM3 (Super-conducting Magnetic Mitigation Method) and material related items has improved the degradation rate of a collector mirror to nearly -0.4%/Billion pulses at 100W level operation. Our schedule is now on time for the 2019 EUV HVM age.

DTCO

Takashi Hisada is a senior research staff member in IBM Research - Tokyo. The title of his report is “Emerging Hardware Technology for Cognitive Computing”. In this report, recent progress of neuromorphic device will be presented. In addition, not just device level integration, but also off-chip packaging level interconnect plays a critical role, so that advanced three-dimensional packaging technology and future hardware concept using recurrent neural network algorithm, which can potentially eliminate the physical dense interconnect, are also introduced.

Jason Cain is currently Principal Member of the Technical Staff. The title of his report is “Design-Technology Co-optimization with Layout Analytics to Meet Scaling Challenges of Advanced Nodes”. In this work a flow for identifying and categorizing such patterns will be described along with methods for integrating the process with the DTCO and product design flows.

Da Yang is responsible for leading node design and process co-optimization supporting Qualcomm flagship mobile SOC chip design, and N+1 node technology definition evaluation. The title of his report is “SoC Scaling Challenges in the Era of Single Digit Technology Nodes”. With the physical dimension scaling path cleared, device innovation and new interconnect material will remain as the bottleneck for 5nm node and beyond. Traditional DTCO has been largely limited to physical design, device, and patterning optimization that in many cases happened in its own area. Future scaling will require better integrated collaborations across design/process/material/tools to overcome the technology challenges and maintain the Moore’s Law.

Ying Li is HXT IC Physical Design Director. The title of his report is “Experience Sharing with Building a Litho-friendly Design of a High-end Server Microprocessor”. In this talk, some experience on how to build a litho-friendly design with the integrated physical design flow is shared.

Srinivas Raghvendra is Vice President of Engineering in Silicon Engineering Group at Synopsys. The title of his report is “Enabling Early and Efficient Technology and Design Choices in Advanced Nodes Through Rigorous Simulations”. In this report, the necessity of concurrent development and optimization of technology/process and design constraints is presented at smaller nodes, both for logic and memory processes. It is also necessary to test the lithography/process constraints thus derived against real layouts and standard cell libraries, not merely test patterns. This talk will describe benefits and details of DTCO based on rigorous simulation and share several practical results.

Dr. Gandharv Bhatara is the Product Marketing Manager for Calibre Semi-Manufacturing. The title of his report is “Design to Silicon: Solving Challenges Connecting Design to Manufacturing at Advanced Nodes with an Integrated Platform”. This talk looks at how we create EDA flows all the way from design to manufacturing that minimize risk, enhance manufacturing, quickly identify & solve issues related to patterning and do it all in a way that allows foundries to minimize their

production costs and turnaround time.

Neeraj Khanna is the Head of Patterning Customer Engagement at KLA-Tencor. The title of his report is "Process Window Discovery and Control for Advanced Design Rules". Traditional lithography process window studies have centered on focus and dose latitudes. However, for sub 14 nm design nodes, engineers have to evaluate a broader set of parameters for new systematic defects on an otherwise centered process.

Optical Microlithography

Stephen D. Hsu is an ASML Fellow and the product lead of imaging product engineering at ASML Brion. The title of his report is "Source Mask Optimization for Advanced Logic and Memory Application". In this report, a SMO flow that provides maximum flexibility for optimizing the source and mask critical layers in the advanced logic and memory process is development. Not only would the optimized source be influenced by the OPC applied to the main feature, but assist feature placement could be included. Current Tachyon SMO supports optimization of the wavefront through FlexWave SMO (DUV only) as well as the target polygons through smart design rule optimization (sDRO). In addition to considering the standard resist effects in modeling the resulting image, SMO has the capability of considering different imaging locations within the resist. With the advent of EUV lithography and its adoption for high volume manufacturing, the greatest challenge in EUV SMO is balancing the traditional imaging metrics of PW, MEEF and PV-Band with the EUV concern of pattern placement error and stochastics. SMO provide the capability of balancing its cost metric to achieve the desired results among all of the imaging metrics of interest. Tachyon SMO has become a technology development platform, widely used in all advanced logic and memory companies; to not only define the imaging source shape, but to explore designs and possible patterning solution and to guide the direction of future designs and enable the scaling roadmap.

Ken Wu is a manage process tech\patterning division at SMIC ATD. The title of his report is "Source-Mask co-Optimization (SMO) Theories and Applications, EUV Simulation Progress and other SMO". In this report, the detail the mechanism in the impact of different source to typical lithographic patterns is studied. Besides, we will present our current learning in the development of EUVL simulation codes and initial results on the 7 nm design rules. Finally, we will present another important subject to every semiconductor engineer under the same short form of SMO, the detail of which will be released during presentation.

Kafai Lai is currently working as a Senior Scientist in the T. J. Watson Research Center at IBM. The title of his report is "From Breaking Optical Diffraction Limit to Breaking Variability Limit in Scaling for Nanoelectronics with Reference to Advanced Patterning". In this talk, a holistic view on the technical aspects of photolithography and the corresponding Design Technology interlock is presented. This talk will touch briefly the variability issues for both computing paradigms, namely both Neumann and non- Von Neumann.

Will Conley is currently in the Applications Engineering Team at Cymer (an ASML company). The title of his report is "Modeling and Experimental Studies on the Imaging Impact of Light Source Bandwidth". In this paper, a methodology for determining the impact that bandwidth variation has on CD dose, focus, pitch and bandwidth will be described in detail to build a dynamic model for further modeling studies and to guide on wafer experiments. This model assists in understanding the impact that bandwidth variability has on the accuracy of the Source and Mask optimization and the overall OPC model. In addition, experimental data demonstrating the process variation through pitch confirming the model built will be presented.

Lithography Solutions

Jan Mulkens is a senior fellow from ASML. The title of his report is “holistic lithography solutions for advanced logic and memory nodes”. First, the holistic optimization architecture needed to support the advanced logic and memory nodes is described. Second, the latest scanner technology which include manipulators for high order control for imaging and overlay is discussed. Third, the latest metrology tool improvements is discussed. Forth, the EPE and illustrate how EPE can be reduced to the required levels are explained. Fifth, the overlay improvement roadmap and show how the latest metrology and computational control methods determine the best recipe for the exposure system is described. Finally, this paper will illustrate how holistic solutions can deal with this.

Dr. Steffen Schulze’s current position is Sr. Director of Marketing for Semiconductor Solutions at Mentor Graphics’ Design to Silicon Division. The title of his report is “Innovations in Computational Lithography Techniques to Enable 7nm and Below”. The presentation will review industry trends enabling further area scaling for integrated circuits – a combination of feature scaling, device and design architecture innovation. Then, the talk will review requirements, highlight EDA solutions and share development trends to continue down this path.